

**What is claimed is:**

1           1.    A method for fabricating a multi-bit vertical memory  
2 cell, comprising:

3           providing a semiconductor substrate having a trench;  
4           forming doped areas, acting as bit lines, in the  
5           semiconductor substrate near its surface and the  
6           bottom of the trench;

7           forming bit line insulating layers over each of the doping  
8           areas;

9           forming a conformable oxide layer over a sidewall of the  
10          trench and the bit line insulating layers to locally  
11          store electric charge; and

12          forming a conducting layer over the insulating layer and  
13          filling in the trench.

1           2.    The method for fabricating a multi-bit vertical  
2 memory cell of claim 1, a fabricating method of the doping  
3 areas further comprising:

4           forming a spacer over the sidewall of the trench; and  
5           performing ion implantation in the substrate using the  
6           spacer as a mask; and  
7           removing the spacer.

1           3.    The method for fabricating a multi-bit vertical  
2 memory cell of claim 2, wherein the spacer is silicon nitride.

1           4.    The method for fabricating a multi-bit vertical  
2 memory cell of claim 2, wherein phosphorous ions are implanted.

1           5.    The method for fabricating a multi-bit vertical  
2 memory cell of claim 1, wherein the bit line insulating layers  
3 are formed by thermal oxidation.

1           6.    The method for fabricating a multi-bit vertical  
2 memory cell of claim 1, wherein the thicknesses of the bit  
3 line insulating layers are 300 to 2000Å.

1           7.    The method for fabricating a multi-bit vertical  
2 memory cell of claim 1, wherein the oxide layer is a silicon  
3 rich oxide layer.

1           8.    The method for fabricating a multi-bit vertical  
2 memory cell of claim 1, wherein the thickness of the oxide  
3 layer is 50 to 110Å.

1           9.    The method for fabricating a multi-bit vertical  
2 memory cell of claim 1, further comprising a gate dielectric  
3 layer between the oxide layer and the trench surface.

1           10.   The method for fabricating a multi-bit vertical  
2 memory cell of claim 9, wherein the gate dielectric layer is  
3 a gate oxide layer.

1           11.   The method for fabricating a multi-bit vertical  
2 memory cell of claim 9, wherein the thickness of the gate  
3 dielectric layer is 50Å.

1           12.   The method for fabricating a multi-bit vertical  
2 memory cell of claim 1, wherein the conducting layer is a poly  
3 layer.

1           13.   A multi-bit vertical memory cell, comprising:

a semiconductor substrate having a trench;  
bit lines formed in the substrate near its surface and  
the bottom of the trench;  
bit line insulating layers disposed over each of the bit  
lines;  
a silicon rich oxide layer conformably formed over a  
sidewall of the trench and the bit line insulating  
layers to locally store electric charge; and  
a word line disposed over the silicon rich oxide layer  
and filled in the trench.

14. The multi-bit vertical memory cell of claim 13,  
wherein the bit lines are formed by phosphorus ion implantation.

15. The multi-bit vertical memory cell of claim 13,  
wherein the thicknesses of the bit line insulating layers are  
300 to 2000Å.

16. The multi-bit vertical memory cell of claim 13,  
wherein the bit line insulating layers are oxide layers.

17. The multi-bit vertical memory cell of claim 13,  
wherein the thickness of the oxide layer is 50 to 110Å.

18. The multi-bit vertical memory cell of claim 13,  
further comprising a gate dielectric layer between the silicon  
rich oxide layer and the trench surface.

19. The multi-bit vertical memory cell of claim 18,  
wherein the thickness of the gate dielectric layer is 50Å.

20. The multi-bit vertical memory cell of claim 13,  
wherein the word line is a poly layer.